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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,038	12/11/2003	Theodore W. Houston	TI-35881	8454

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EXAMINER

LE, THONG QUOC

ART UNIT PAPER NUMBER

2827

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,038	HOUSTON, THEODORE W.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,5-10 and 12-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,5,9,10,12-16,20 and 21 is/are rejected.
- 7) ☒ Claim(s) 6-8,17-19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Amendment filed on 07/19/2006 has been entered.
2. Claims 1,5-10,12-21 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1,5-10,12-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,5,9-10,12-16,20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Inaba (U.S. Patent No. 6,137,732).

Regarding claim 1, Inaba discloses an SRAM device (Figure 1), comprising:

an SRAM array (3) coupled to row peripheral circuitry (4) by a word line (Figure 11, WL) and coupled to column peripheral circuitry (5) by bit lines (Figure 11, D, DB);
and

an array low voltage control circuitry (Figure 7, Column 5, lines 18-21, lines 32-42, Figures 6, Column 10, lines 45-49, four voltages) that provides an enhanced low operating voltage V_{ESS} to said SRAM array during at least a portion of a READ operation or a WRITE operation (Column 10, lines 3-5, write data with a low voltage

VBB) thereof, said enhanced low operating voltage VESS having a higher value than a low operating voltage Vss (Figures 6, Vbb higher than Vss (Vcc) Column 10, lines 1-5, lines 34-54, Column 12, lines 19-29, Column 12, lines 43-52).

Regarding claim 5, Inaba discloses wherein said array low voltage control circuitry provides said enhanced low operating voltage VESS based on a factor selected from the group consisting of: a process corner, a transistor parameter, a mode of operation, and a value of a high supply voltage (Column 8, lines 12-21, Column 9, lines 1-5, WCE , mode of write operation).

Regarding claim 10, Inaba discloses wherein said array low voltage control circuitry provides said enhanced low operating voltage VESS employing a component selected from the group consisting of: a diode, a transistor, a fuse, a ROM, a voltage regulator, and logic circuitry (Figure 1, 2).

Regarding claim 12, Inaba discloses a method of operating an SRAM device (Figure 1) , comprising: employing in an integrated circuit an SRAM array (Figure 1, 3) coupled to row peripheral circuitry (4) by a word line and coupled to column peripheral circuitry (5) by bit lines; and providing an enhanced low operating voltage VESS to said SRAM array during at least a portion of an active mode, said enhanced low operating voltage VESS having a higher value than a low operating voltage Vss (Figures 6, Vbb higher than Vss (Vcc) Column 10, lines 1-5, lines 34-54, Column 12, lines 19-29, Column 12, lines 43-52).

Regarding claims 13-15, 18, Inaba discloses wherein said providing only occurs during a WRITE operation (Column 2, lines 7-11, Column 10, lines 27-33), and wherein

said providing occurs during all of said active mode (Column 1, lines 64-67, Column 2, lines 1-11, Column 10, lines 27-33), and wherein said providing occurs during all modes (Column 1, lines 64-67, Column 2, lines 1-11, Column 10, lines 27-33), and wherein said providing is based on a factor selected from the group consisting of: a process corner, a transistor parameter, a mode of operation, and a value of a high supply voltage (Column 8, lines 18-22, WCE mode).

Regarding claims 20-21, Inaba discloses wherein said providing includes employing an active component (Figure 2, WCE) to provide said enhanced low operating voltage V_{ESS}, and wherein said providing includes employing a component selected from the group consisting of: a diode, a transistor, a fuse, a ROM, a voltage regulator, and logic circuitry (Figure 1,2).

Allowable Subject Matter

6. Claims 6-8, 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-8, 17-19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Inaba (U.S. Patent No. 6,137,732), and others, does not teach the claimed invention having wherein the array low voltage control circuitry provides the enhanced low operating V_{ESS} at a higher value when based on a strong n process

corner, and Vess at a lower value during the READ operation than during a WRITE operation.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2827

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Thong Q. Le
Primary Examiner
Art Unit 2827

9/18/2006